

## MSM5840

### CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

#### GENERAL DESCRIPTION

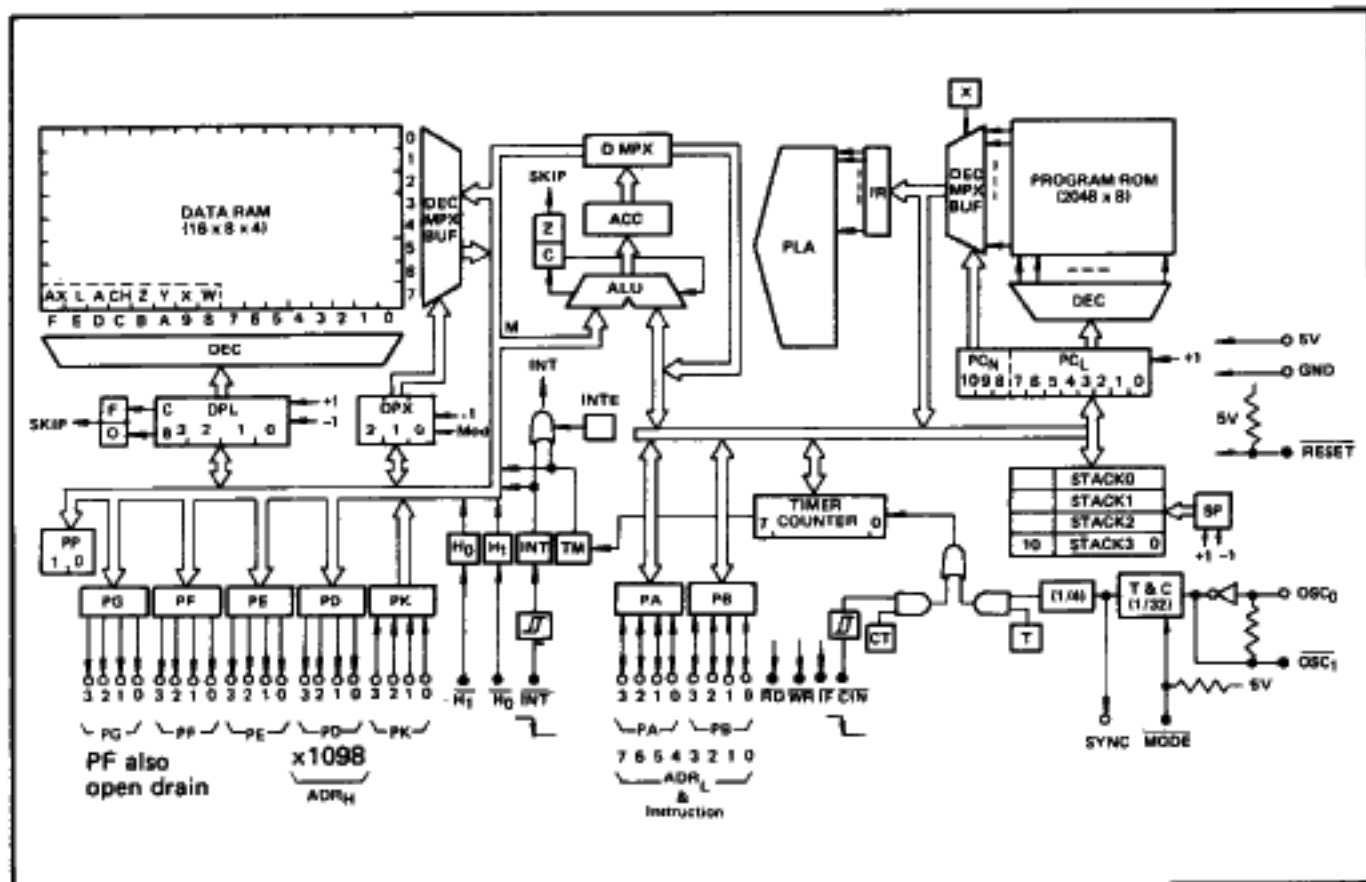
The OKI MSM5840 microcontroller is a low-power, high-performance single chip device implemented in complementary metal oxide semiconductor technology. Integrated within this one chip are 16K bits of mask program ROM, 512 bits of data RAM, 30 Input/Output lines, a programmable timer/counter, and oscillator. Program memory is byte wide and data-paths are organized in 4 bit nibbles. RAM and I/O lines are bit addressable. Up to 4K of external ROM interfaces to the 8 bit bidirectional bus. 98 instructions include binary, BCD, logical operations; bit set, reset, test, 8 bit I/O; relative jumps; multifunctional instructions (increment, modify, skip); 8 bit wide table output; subroutine call and return. 94% of instructions are single byte, single cycle operations.

#### FEATURES

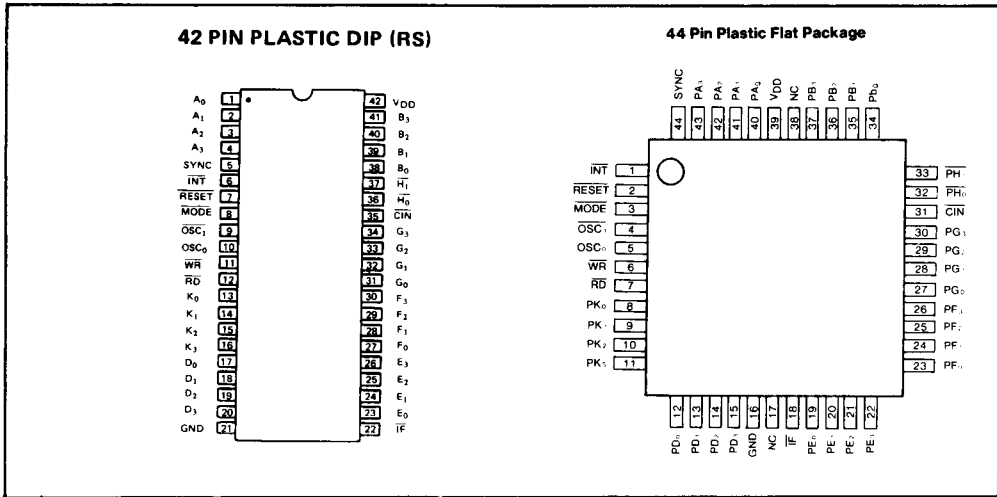
- Low Power Consumption – 8mW Typical
- 100% Static Logic – 50 $\mu$ W Standby, Typical
- 2K  $\times$  8 Internal ROM
- Up to 4K  $\times$  8 External ROM
- 128  $\times$  4 Internal RAM
- 30 I/O Lines Incl. 8 Bit Data Bus
- Programmable 8 Bit Timer/Counter
- Self-contained Oscillator
- 98 Instructions
- Expandable Memory and I/O
- 2 Interrupt Levels
- 4 Stack Levels
- Operating Temperature –40° to +85°C
- 3V to 6V Operating V<sub>DD</sub>
- Battery Powered or Battery Backup
- TTL Compatible (with pullups)
- 7.6 $\mu$ s Cycle Time @4.2MHz (V<sub>DD</sub> 5V $\pm$  10%)

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#### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION (Top View)



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## PIN DESCRIPTION

Designation	Pin No.	Function
GND	21	Circuit GND potential
V <sub>DD</sub>	42	Main power source (+5V)
OSC <sub>0</sub>	10	Crystal OSC input, external clock input
OSC <sub>1</sub>	9	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	1 to 4 38 to 41	Pseudo-bidirectional ports for 4-bit parallel I/O. Used as a pair for 8-bit I/O. Used to output 8 LSBs of address in external ROM mode. Used to read external instruction during IF.
PD, PE, PE, PG	17 to 20 23 to 34	Output ports for 4-bit parallel output and bit set/reset. Specified by internal port pointer, Bit position specified by set/reset instruction. PD also used for instruction address MSBs in external ROM mode during IF.
PK	13 to 16	4-bit parallel or bit test input port (unlatched)
PH	36 and 37	2-bit input port with latched memory (negative level sensitive)
RESET	7	RESET has priority over every other signal. (see MSM5840 user's manual for initialization sequence)
MODE	8	Used to enable external ROM mode during RESET and also to enable STOP mode during execution (for stepping program)
INT	6	Negative edge sensitive external interrupt signal associated with EI and DI instructions. Vectors to location 200H.
CIN	35	Negative edge sensitive external input for counter associated with ECT and DCT instructions. Vectors to location 100H. (same as timer)
SYNC	5	General purpose synchronizing signal output at the beginning of each machine cycle. Used for address strobe during external ROM mode.
RD	12	Read strobe pulse occurring when port A or B is read (1A, 1B, 1AB)
WR	11	Write strobe pulse occurring when port A or B is written (OA, OB, OAB, OBS, OTD)
IF	22	Read strobe pulse occurring during an instruction fetch from external ROM.

## FUNCTIONAL DESCRIPTION

### Program ROM

The MSM5840 will address up to 4K bytes of program ROM and can have 2K bytes of internal masked ROM, or all ROM may be located externally. External EPROM may be used for program development with conversion to internal ROM occurring after program debug and system check-out and verification. All instructions are byte wide. Only three of the 98 instructions require two bytes of program code. The instructions are routed to a programmed logic array which generates the necessary internal control signals.

### Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 128 nibbles, 8 nibbles of which are dedicated registers accessible directly under program control. These are the general purpose registers, W, X, Y and Z, and the 4 save (exchange) registers, CH, A, L, and AX. All other DATA RAM must be addressed indirectly through the DP (data pointer) registers, a seven bit pointer (directly accessible by numerous instructions) consisting of 4 bit DPL register and a 3 bit DP<sub>H</sub> register. Any nibble of internal data RAM can be accessed through the DP registers. Some instructions automatically change the contents of the DP registers allowing efficient array processing.

### Input/Output Ports

PA, PB – These two ports are pseudo-bidirectional ports which can be used as simple I/O lines or used as either a 4-bit or 8-bit parallel bus. An instruction fetches the external ROM data through these ports by outputting the 8 low order bits of address during SYNC followed by an IF (instruction fetch) cycle. In addition, synchronized data transfers are possible through these ports with the I/O pin signals  $\overline{RD}$  and  $\overline{WR}$  associated with certain input/output instructions dedicated to these ports. In short, PA and PB can be used as a multiplexed address/instruction/data bus.

PD, PE, PF, PG – These four output ports are addressed indirectly through the TWO BIT port pointer whose contents are changed through certain instructions. These ports are bit (set/reset) addressable. PD is also used for the high order bits of address during an external instruction fetch. PF and PG are open drain outputs and PG is set high by a hardware RESET.

PK is an input port without memory, addressable either as a nibble or bit level input.

PH is a two-bit input port with memory, which can be tested and reset under program control.

### External Interrupt

The INT pin can be tested under program control or enabled to cause a vectored interrupt to location 200H. It is negative edge sensitive.

### Timer/Counter

The timer/counter is an 8-bit counter whose input is selected under program control to be either an external signal (CIN) or an internal square wave of 1/128 the frequency of the OSC<sub>0</sub> input ( $2 \text{ MHz}/128 = 15.625 \text{ kHz}$ ). The timer/counter can be enabled or disabled under program control as can be associated internal interrupt which vectors to location 100H and has higher priority than the external interrupt.

### Stack

The stack is an LIFO queue for storing return-from-interrupt and return-from-subroutine address information. It is eleven bits wide and 4 levels deep.

### Program Counter (PC)

The program counter is 11 bits wide and loaded under program control.

### Accumulator

The accumulator register is the data path focal point of the CPU. Approximately one-half of the instructions involve the accumulator. Its contents are the source and destination for many ALU operations and port operations. CASE statements (computed GOTOS) are possible by using the Jump with Accumulator (JA) instruction.

### Flags

The MSM5840 is endowed with the following set of flags.

Z – zero flag	:	Indicates that the result of the previous operation was zero
F – all ones	:	Indicates a carry from the DP <sub>L</sub> register
O – all zeros	:	Indicates a borrow from the DP <sub>L</sub> register
C – carry	:	Indicates a carry from the previous operation
T – timer	:	Indicates that the timer/counter is specified as a timer
CT – counter	:	Indicates that the timer/counter is specified as a counter
TM – timer flag	:	Indicates an overflow of the timer/counter register
INT – interrupt	:	Latching memory flag for the external interrupt
INTE – interrupt enable	:	Indicates that interrupts have been enabled
H <sub>0</sub> – H <sub>0</sub> memory	:	Indicates that an input has been detected on the H <sub>0</sub> input
H <sub>1</sub>	:	same as H <sub>0</sub> except H <sub>1</sub> input
X	:	0 indicates internal ROM, 1 indicates external ROM. If all external ROM, 0 indicates first bank of 2K.

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## INSTRUCTION SET

Mnemonic	Description	Instruction Code								Byte	Cycle	
		7	6	5	4	3	2	1	0			
Load, Store, Read, Clear	CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
	CLL	Clear DP <sub>L</sub>	0	0	1	0	0	0	0	0	1	1
	CLH	Clear DP <sub>H</sub>	0	1	1	0	0	0	0	0	1	1
	LAI	Load Accumulator with Immediate	0	0	0	1	<i>l<sub>3</sub></i>	<i>l<sub>2</sub></i>	<i>l<sub>1</sub></i>	<i>l<sub>0</sub></i>	1	1
	LLI	Load DP <sub>L</sub> with Immediate	0	0	1	0	<i>l<sub>3</sub></i>	<i>l<sub>2</sub></i>	<i>l<sub>1</sub></i>	<i>l<sub>0</sub></i>	1	1
	LHI	Load DP <sub>H</sub> with Immediate	0	1	1	0	0	<i>l<sub>2</sub></i>	<i>l<sub>1</sub></i>	<i>l<sub>0</sub></i>	1	1
	L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
	LM	Load Accumulator with Memory then Modify DP <sub>H</sub>	1	0	0	1	0	1	<i>l<sub>1</sub></i>	<i>l<sub>0</sub></i>	1	1
	LAL	Load Accumulator with DP <sub>L</sub>	0	1	0	1	0	1	0	1	1	1
	LLA	Load DP <sub>L</sub> with Accumulator	0	1	0	1	0	1	0	0	1	1
	LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
	LAX	Load Accumulator with X Register	1	0	0	0	0	1	0	1	1	1
	LAY	Load Accumulator with Y Register	1	0	0	0	0	1	1	0	1	1
	LAZ	Load Accumulator with Z Register	1	0	0	0	0	1	1	1	1	1
	SI	Store Accumulator to Memory then Increment DP <sub>L</sub>	1	0	0	1	0	0	0	0	1	1
	SMI	Store Accumulator to Memory then Modify DP <sub>H</sub> and Increment DP <sub>L</sub>	1	0	0	1	0	0	<i>l<sub>1</sub></i>	<i>l<sub>0</sub></i>	1	1
	LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
	LXA	Load X Register with Accumulator	1	0	0	0	0	0	0	1	1	1
	LYA	Load Y Register with Accumulator	1	0	0	0	0	0	1	0	1	1
	LZA	Load Z Register with Accumulator	1	0	0	0	0	0	1	1	1	1
LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1	
LTl	Load Timer with Immediate	0	1	1	0	1	0	0	0	2	2	
RTH	Read Timer H	0	1	1	0	1	0	1	0	1	1	
RTL	Read timer L	0	1	1	0	1	0	1	1	1	1	
Exchange	XA	Exchange Accumulator with Save Register A	0	1	0	0	1	0	0	1	1	1
	XL	Exchange DP <sub>L</sub> with Save Register L	0	1	0	0	1	0	1	0	1	1
	XCH	Exchange DP <sub>H</sub> and Carry with Save Register CH	0	1	0	0	1	0	0	0	1	1
	X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
	XM	Exchange Accumulator with Memory then Modify DP <sub>H</sub>	1	0	0	1	1	0	<i>l<sub>1</sub></i>	<i>l<sub>0</sub></i>	1	1
	XAX	Exchange Accumulator with Save Register AX	0	1	0	0	1	0	1	1	1	1
Increment/Decrement	INA	Increment Accumulator	0	0	0	0	0	0	0	1	1	1
	INL	Increment DP <sub>L</sub>	0	1	0	1	0	1	1	1	1	1
	INM	Increment Memory	0	1	0	1	1	1	0	1	1	1
	INW	Increment W Register	1	0	0	0	1	0	0	0	1	1
	INX	Increment X Register	1	0	0	0	1	0	0	1	1	1
	INY	Increment Y Register	1	0	0	0	1	0	1	0	1	1
	INZ	Increment Z Register	1	0	0	0	1	0	1	1	1	1

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**INSTRUCTION SET (CONT.)**

Mnemonic	Description	Instruction Code								Byte	Cycle	
		7	6	5	4	3	2	1	0			
Increment/Decrement	DCA	Decrement Accumulator – Skip if Not All Ones	0	0	0	0	1	1	1	1	1	1
	DCL	Decrement DP <sub>L</sub>	0	1	0	1	0	1	1	0	1	1
	DCM	Decrement Memory	0	1	0	1	1	1	0	0	1	1
	DCW	Decrement W Register	1	0	0	0	1	1	0	0	1	1
	DCX	Decrement X Register	1	0	0	0	1	1	0	1	1	1
	DCY	Decrement Y Register	1	0	0	0	1	1	1	0	1	1
	DCZ	Decrement Z Register	1	0	0	0	1	1	1	1	1	1
	DCH	Decrement DP <sub>H</sub> – Skip if All Ones and C = Zero	0	1	0	1	1	1	1	1	1	1
Logical	CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
	AND	And Accumulator with Memory	0	1	0	0	0	1	0	0	1	1
	OR	Or Accumulator with Memory	0	1	0	0	0	1	0	1	1	1
	EOR	Exclusive or Accumulator with Memory	0	1	0	0	0	1	1	0	1	1
	RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
Arithmetic	AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
	ACS	Add Memory to Accumulator with Carry, Skip if Carry	0	1	0	0	1	1	0	1	1	1
	AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	1	0	1	1
	AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	<i>l</i> <sub>3</sub>	<i>l</i> <sub>2</sub>	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
	CM	Compare Accumulator with Memory, Skip if Equal	0	1	0	1	1	1	1	0	1	1
	AWS	Add W Register to Accumulator, Skip if Carry	1	0	0	1	1	1	0	0	1	1
	AXS	Add X Register to Accumulator, Skip if Carry	1	0	0	1	1	1	0	1	1	1
	AYS	And Y Register to Accumulator, Skip if Carry	1	0	0	1	1	1	1	0	1	1
AZS	Add Z Register to Accumulator, Skip if Carry	1	0	0	1	1	1	1	1	1	1	
Bit Set/Reset/Test	SPB	Set Port Bit	1	0	1	1	0	0	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	RPB	Reset Port Bit	1	0	1	1	0	1	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	SMB	Set Memory Bit	1	0	1	1	1	0	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	RMB	Reset Memory Bit	1	0	1	1	1	1	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	TAB	Test Accumulator Bit	1	0	1	0	0	0	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	TMB	Test Memory Bit	1	0	1	0	0	1	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	TKB	Test K Port Bit	1	0	1	0	1	0	<i>l</i> <sub>1</sub>	<i>l</i> <sub>0</sub>	1	1
	THB	Test H Port Bit	1	0	1	0	1	1	<i>l</i> <sub>0</sub>		1	1
	TI	Test Interrupt flag	1	0	1	0	1	1	1	1	1	1
	TTM	Test Time flag	1	0	1	0	1	1	1	0	1	1
	TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
	SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
	RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1

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**INSTRUCTION SET (CONT.)**

Mnemonic	Description	Instruction Code								Byte	Cycle	
		7	6	5	4	3	2	1	0			
Branch/Subroutine	J	Jump	0	0	1	1	0	l <sub>10</sub>	l <sub>9</sub>	8	2	2
	JC	Jump in Current Page	1	1	l <sub>5</sub>	l <sub>4</sub>	l <sub>3</sub>	l <sub>2</sub>	l <sub>1</sub>	l <sub>0</sub>	1	1
	JA	Jump with Accumulator	0	1	0	0	0	0	1	1	1	1
	CAL	Call Subroutine	0	0	1	1	1	l <sub>10</sub>	l <sub>9</sub>	8	2	2
	RT	Return from Subroutine	0	1	0	1	1	0	0	1	1	2
Input/Output	OBS	Output Byte String	0	1	1	1	0	0	0	0	1	2~17
	OTD	Output Table Data	0	1	1	1	0	0	0	1	1	2
	OA	Output Accumulator to Port A	0	1	1	1	0	0	1	0	1	1
	OB	Output Accumulator to Port B	0	1	1	1	0	0	1	1	1	1
	OP	Output Accumulator to Port P designated Port Pointer	0	1	1	1	0	1	0	0	1	1
	OAB	Output Memory and Accumulator to Ports A and B	0	1	1	1	0	1	0	1	1	1
	OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
	IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
	IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
	IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
IAB	Input Ports A and B in Memory and Accumulator	0	1	1	1	1	0	1	1	1	1	
Control	EI	Enable Interrupt	0	1	0	1	0	0	1	1	1	1
	DI	Disable Interrupt	0	1	0	1	0	0	1	0	1	1
	ET	Enable Timer	0	1	1	0	1	1	1	1	1	1
	DT	Disable Timer	0	1	1	0	1	1	1	0	1	1
	ECT	Enable Counter	0	1	1	1	1	1	1	1	1	1
	DCT	Disable Counter	0	1	1	1	1	1	1	0	1	1
	HLT	Halt	0	1	1	0	1	1	0	1	1	1
	EXP	Exchange Program	0	1	1	0	1	0	0	1	1	1
NOP	No Operation	0	0	0	0	0	0	0	0	1	1	

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## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V <sub>DD</sub>	T <sub>a</sub> = 25°C	-0.3 to 7	V
Input Voltage	V <sub>I</sub>	T <sub>a</sub> = 25°C	-0.3 to V <sub>DD</sub>	V
Operating Voltage PF PG	V <sub>O</sub>	T <sub>a</sub> = 25°C	-0.3 to 25	V
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

**Note:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## OPERATING CONDITIONS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V <sub>DD</sub>	@ 1 MHz	3 to 6	V
		@ 4.2 MHz	4.5 to 5.5	V
Operating Temperature	T <sub>op</sub>		-40 to +85	°C
Fan Out	N	MOS Load	15	
		TTL Load	1	

## D.C. CHARACTERISTICS

(V<sub>DD</sub> = 5V ± 10%, T<sub>a</sub> = -20° to +70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Input Voltage	V <sub>IH</sub>	-	3.6			V
Low Input Voltage	V <sub>IL</sub>	-			0.8	V
High Output Voltage <sup>(1)</sup>	V <sub>OH</sub>	I <sub>O</sub> = -40μA	4.2			V
Low Output Voltage	V <sub>OL</sub>	I <sub>O</sub> = 1.6mA			0.4	V
OSC <sub>0</sub> Input Leak Current	I <sub>IH</sub>	V <sub>I</sub> = V <sub>DD</sub> /0V			25	μA
	I <sub>IL</sub>				-25	
RESET, MODE Leak Current	I <sub>IH</sub>	V <sub>I</sub> = V <sub>DD</sub> /0V			1	μA
	I <sub>IL</sub>				-50	
Input Leak Current <sup>(2)</sup>	I <sub>IH</sub>	V <sub>I</sub> = V <sub>DD</sub> /0V			1	μA
	I <sub>IL</sub>				-1	
PA, PB High Output Current	I <sub>OH</sub>	V <sub>OH</sub> = 0.4V			-1	mA
High Output Current <sup>(1)</sup>	I <sub>OH</sub>	V <sub>OH</sub> = 2.5V	-0.25			mA
Low Output Current	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V	1.6			mA
PF, PG Output Breakdown Voltage	BV <sub>OH</sub>	I <sub>O</sub> = 10μA	20			V
Input Capacitance	C <sub>I</sub>	f = 1MHz T <sub>a</sub> = 25°C		5		pF
Output Capacitance	C <sub>O</sub>	f = 1MHz T <sub>a</sub> = 25°C		7		pF
Current Consumption <sup>(3)</sup>	I <sub>DD</sub>	V <sub>I</sub> = V <sub>DD</sub> /0V		10	200	μA
	I <sub>DD</sub>	V <sub>I</sub> = V <sub>DD</sub> /0V f = 4.2MHz		1.6	4	mA

**Notes:** (1) Except PA, PB (see graphs)  
 (2) Except OSC<sub>0</sub>, RESET, MODE  
 (3) Typical Value of V<sub>DD</sub> is 5V

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**A.C. CHARACTERISTICS (INTERNAL ROM MODE)**

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -40^\circ$  to  $+85^\circ C$ )

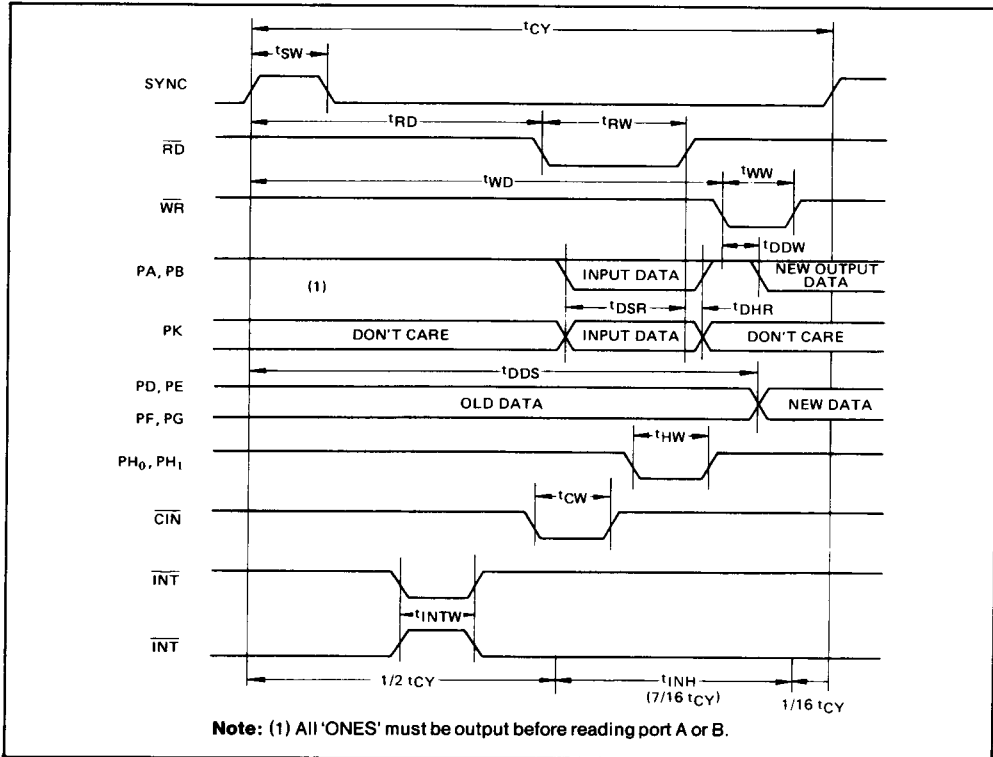
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	$t_{CY}$		7.6			$\mu S$
Sync Pulse Width	$t_{SW}$		0.95			$\mu S$
$\overline{RD}$ Pulse Width	$t_{RW}$		1.9			$\mu S$
Sync $\uparrow$ to $\overline{RD}$ $\downarrow$	$t_{RD}$	$C_L = 50pF$	$1/2 t_{CY} + 0.5$			$\mu S$
$\overline{WR}$ Pulse Width	$t_{WW}$		0.95			$\mu S$
Sync $\uparrow$ to $\overline{WR}$ $\downarrow$	$t_{WD}$	$C_L = 50pF$	$13/16 t_{CY} + 0.5$			$\mu S$
Port Input Setup Time	$t_{DSR}$		$4/16 t_{CY}$			$\mu S$
Port Input Hold Time	$t_{DHR}$		0		0.8	$\mu S$
$\overline{WR}$ $\downarrow$ to New Data Valid	$t_{DDW}$	PA, PB $C_L = 50pF$			0.8	$\mu S$
Sync $\uparrow$ to New Data Valid	$t_{DDS}$	PD, PE, PF, PG $C_L = 50pF$			$13/16 t_{CY} + 0.5$	$\mu S$
PH <sub>0</sub> , PH <sub>1</sub> Input Pulse Width	$t_{HW}$	(1)	500			nS
$\overline{CIN}$ Input Pulse Width	$t_{CW}$		250			nS
INT Input Pulse Width	$t_{INTW}$	(1)	500			nS

**Note:** (1) The processor logic will ignore the following events:

1. An INT falling edge occurring during  $T_{INH}$  of a  $T_I$  instruction.
2. A PH<sub>0</sub> or PH<sub>1</sub> low level occurring only during  $T_{INH}$  of a  $T_{HB}$  instruction.

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**TIMING CHARTS**

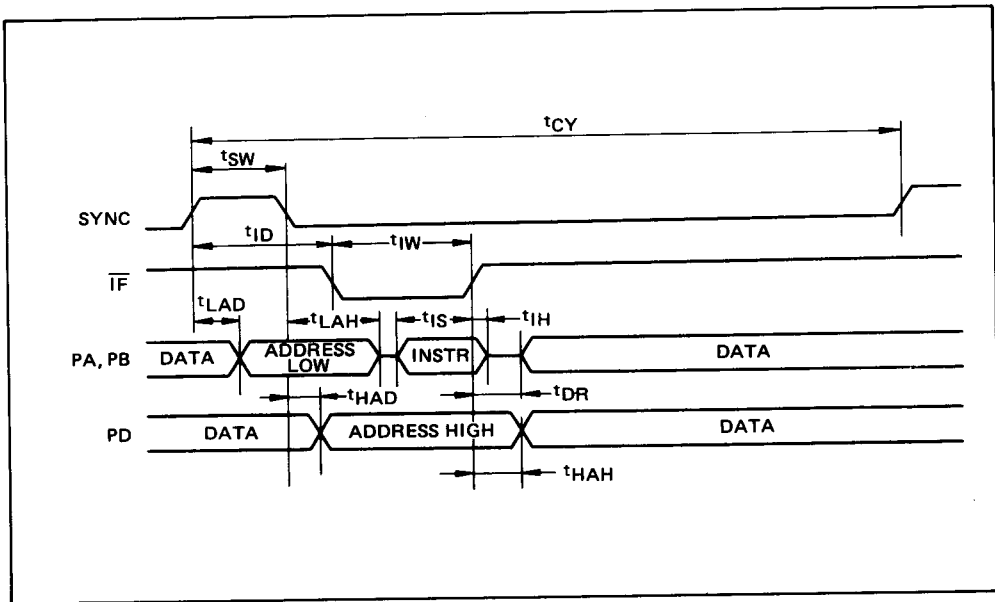




### A.C. CHARACTERISTICS (EXTERNAL ROM MODE)

(VDD = 5V±10%, Ta = -40° to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t <sub>CY</sub>		7.6			μS
Sync Pulse Width	t <sub>SW</sub>		0.95			μS
IF Pulse Width	t <sub>IW</sub>		1.425			μS
Sync ↑ to IF ↓	t <sub>ID</sub>	C <sub>L</sub> = 50pF	3/16 t <sub>CY</sub> + 1			μS
Address Low Delay	t <sub>LAD</sub>	C <sub>L</sub> = 50pF			0.8	μS
Address Low Hold	t <sub>LAH</sub>		1/16 t <sub>CY</sub>		1/16 t <sub>CY</sub> +1	μS
Instruction Setup	t <sub>IS</sub>		1/16 t <sub>CY</sub>			μS
Instruction Hold	t <sub>IH</sub>				20	nS
Data Recovery	t <sub>DR</sub>	C <sub>L</sub> = 50pF	0		0.8	μS
Address High Delay	t <sub>HAD</sub>	C <sub>L</sub> = 50pF			0.5	μS
Address High Hold	t <sub>HAH</sub>		0		0.5	μS



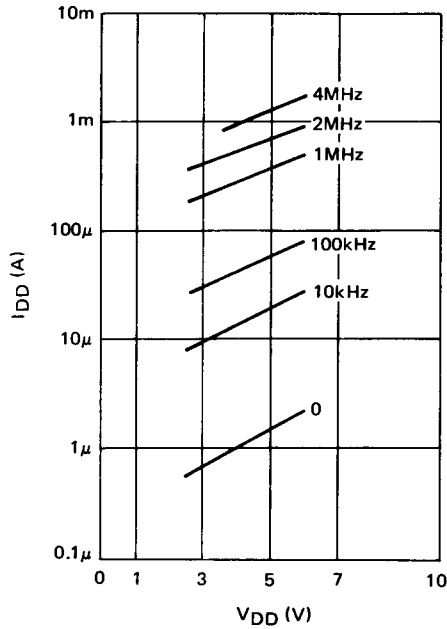
6

Cycle Dependent Timings	4MHz	2MHz	1MHz	500kHz
1/16t <sub>CY</sub>	0.5μS	1μS	2μS	4μS
1/16t <sub>CY</sub> +1	1.5μS	2μS	3μS	5μS
3/16t <sub>CY</sub> +1	2.5μS	4μS	7μS	13μS
4/16t <sub>CY</sub> -1	1μS	3μS	7μS	15μS
1/2t <sub>CY</sub> +1	5μS	9μS	17μS	33μS
7/16t <sub>CY</sub>	3.5μS	7μS	14μS	28μS
13/16t <sub>CY</sub> +1	7.5μS	14μS	27μS	53μS

## TYPICAL PERFORMANCE CURVES

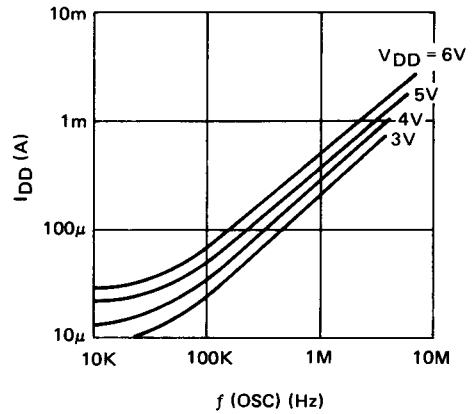
**Supply Current vs Supply Voltage**

( $T_a = 25^\circ\text{C}$ , No Load)



**Supply Current vs Oscillator Frequency**

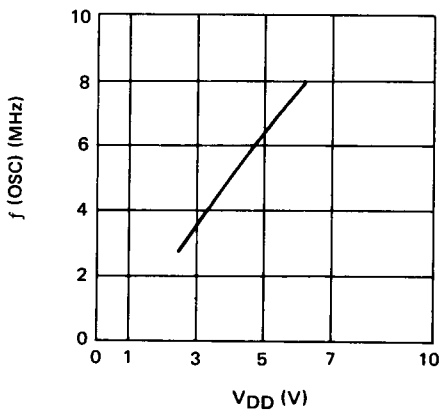
( $T_a = 25^\circ\text{C}$ , No Load)



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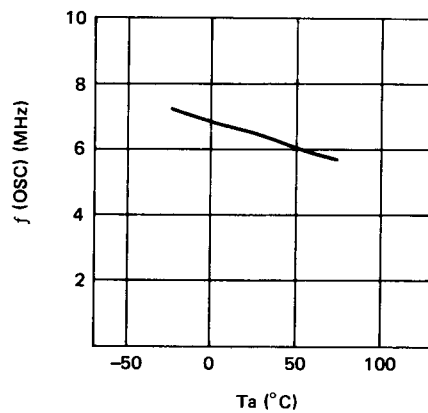
**Oscillator Frequency vs Supply Voltage**

( $T_a = 25^\circ\text{C}$ ,  $C_L = 50\text{pF}$ )

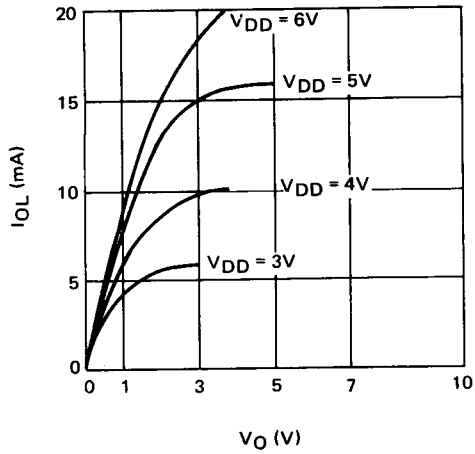


**Oscillator Frequency vs Temperature**

( $C_L = 50\text{pF}$ )

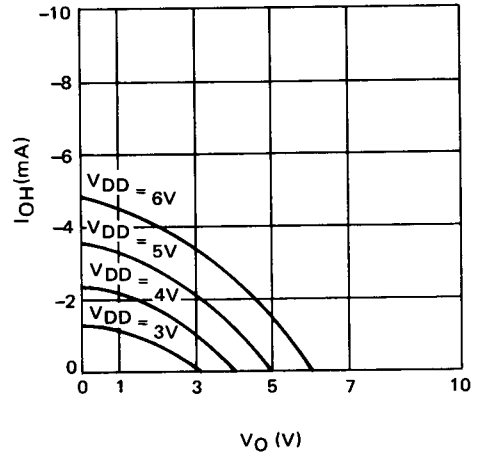


**Low Current Out vs Voltage**



**High Current Out vs Voltage**

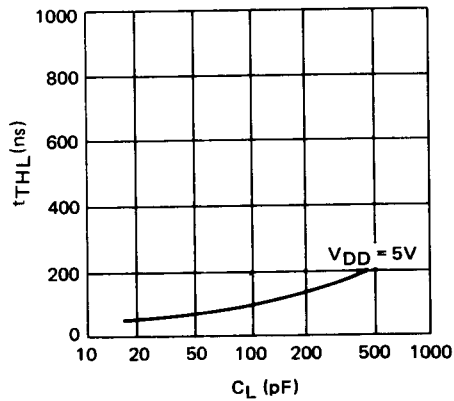
( $T_a = 25^\circ C$ , Except PA, PB)



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**Fall Time vs Load**

( $T_a = 25^\circ C$ , PA, PB, PD, PE,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{IF}$ , SYNC)



**Rise Time vs Load**

( $T_a = 25^\circ C$ , PD, PE,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{IF}$ , SYNC)

