



DESCRIPTION

The AP8022 consists of a Pulse Width Modulator (PWM) controller and a power MOSFET, specifically designed for a high performance off-line converter with minimal external components. AP8022 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over temperature protection (OTP), under-voltage Lockout protection(UVLO) , V_{DD} over-voltage protection(OVP), and soft-start. Burst mode operation and device very low consumption helps to meet the standby energy saving regulations. Excellent EMI performance is achieved with frequency modulation. The device consists of a high voltage start-up circuit in order to reduce the system set-up time. The device provides an advanced platform well suited for low standby-power and cost-effective flyback converters.

The AP8022 is available in DIP8 package.

ORDERING INFORMATION

Package Type	Part Number	
DIP8	P8	AP8022P8U
		AP8022P8VU
Note	V: Halogen free Package U: Tube SPQ: 50pcs/Tube	
AiT provides all RoHS products Suffix " V " means Halogen free Package		

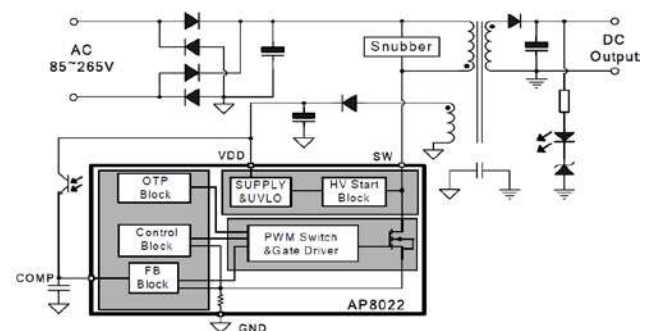
FEATURES

- Integrated 800V avalanche-rugged power MOSFET
- 85V to 265V wide range AC voltage input
- Semi enclosed steady output power
10W@85~265V_{AC}
- Frequency modulation for low EMI
- Burst-mode Operation
- Built-in Soft Start
- Internal HV Start-up Circuit
- Excellent Protection:
Over Current Protection (OCP)
Over Temperature Protection (OTP)
 V_{DD} over-voltage protection (OVP)
- Available in DIP8 Package

APPLICATION

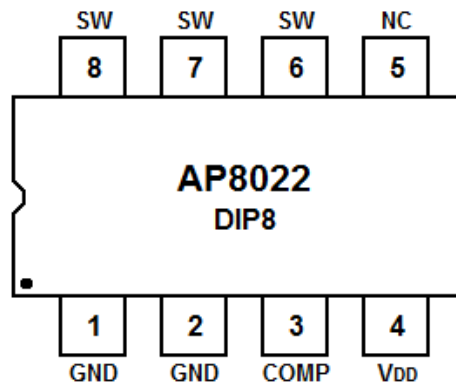
- Electromagnetic Oven power supplies
- Small household application power supplies
- DVB/DVD Power

TYPICAL APPLICATION





PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1, 2	GND	Ground
3	COMP	Voltage feedback. By connecting a opto-coupler to close the control loop and achieve the regulation.
4	V _{DD}	Positive Supply voltage Input.
5	NC	No connection
6,7,8	SW	The SW pin is designed to connect directly to the primary lead of the transformer.

TYPICAL POWER

Package	AC line	continuous power ^{NOTE1}	Peak power ^{NOTE2}
DIP8	85~265 V _{AC}	10W(12V 800mA)	12W(12V 1A)

NOTE1: Maximum output power in a semi enclosed design measured at 75°C ambient temperature, Duration:2 hours

NOTE2: Peak power in a semi enclosed design measured at 75°C ambient temperature, Duration:1 min



ABSOLUTE MAXIMUM RATINGS

Supply voltage Pin V _{DD}	-0.3V~45V	
High-Voltage Pin, SW	-0.3V~750V	
COMP	-0.3V~7V	
Junction Temperature	-40°C~150°C	
Storage Temperature	-55°C~150°C	
Lead Temperature (Soldering, 10secs)	260°C	
Package Thermal Resistance	DIP8	40°C/W
Electrostatic Discharge Human Body Mode (HBM, ESDA/JEDEC JDS-001-2014)	±4kV	
ESD Voltage Protection ^{NOTE3} (Air discharge to pins of AP8022 with ESD Generator)	8kV	
Drain Pulse Current (T _{pulse} =100μs)	3A	

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE3: Enterprise internal standards, for reference only.

ELECTRICAL CHARACTERISTICS

T_J =25°C, V_{DD} = 15 V, unless otherwise specified

Power section

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
VDMOS Breakdown Voltage	B _{VDS}	I _{SW} =250μA	750	800		V
Static Drain-Source off Current	I _{OFF}	V _{SW} =550V			100	μA
Static Drain-Source on Resistance	R _{DS(on)}	I _{SW} = 400mA, T _J =25°C		10		Ω

Control section

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
UVLO SECTION						
V _{DD} Start Threshold Voltage	V _{START}	V _{COMP} =0V	13	14.5	16	V
V _{DD} Stop Threshold Voltage	V _{STOP}	V _{COMP} =0V	7	8	9	V
V _{DD} Threshold Hysteresis	V _{HYS}			6.5		V
V _{DD} Reset Voltage	V _{RST}		5.5	6	6.5	V

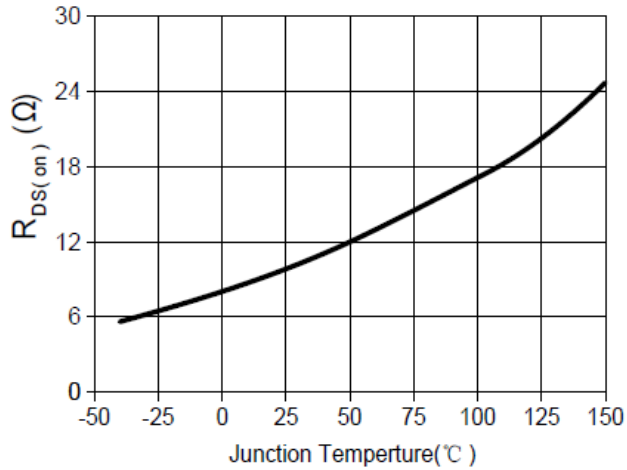


Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
OSCILLATOR SECTION						
Initial Accuracy	F _{OSC}	T _A = 25°C	54	60	66	kHz
Frequency Variation	FD			±6		kHz
Modulation Frequency	FM			250		Hz
Maximum Duty Cycle	D _{MAX}		65	80	90	%
FEEDBACK SECTION						
Feedback Shutdown Current	I _{COMP}			1.2		mA
COMP Pin Input Impedance	R _{COMP}			1.15		kΩ
CURRENT LIMIT SECTION						
Peak Current Limit	I _{LIM}	T _A = 25°C	0.6	0.75	0.9	A
Minimum Turn On Time	t _{LEB}	LEB time		650		ns
Soft-start Time	t _{SS}			7.5		ms
Peak Drain Current During Burst Mode	I _{D_BM}			150		mA
PROTECTION SECTION						
Thermal Shutdown Temperature	T _{SD}		140	170		°C
Thermal Shutdown Hysteresis	T _{HYST}			30		°C
SUPPLY CURRENT SECTION						
Startup Charging Current (SW pin)	I _{CH}	V _{DRAIN} = 105V, V _{COMP} = GND, V _{DD} = 12V		-1.25		mA
Operating Supply Current, Switching	I _{DD}	V _{DD} = 16V, V _{COMP} = 0V		4		mA
Operating Voltage Range	V _{DD}	After turn-on	10		35	V
V _{DD} Over Voltage	V _{OVP}		37	40	43	V
Operating Supply Current with V _{DD} < V _{STOP}	I _{DD_OFF}	V _{DD} = 6V	100		400	μA

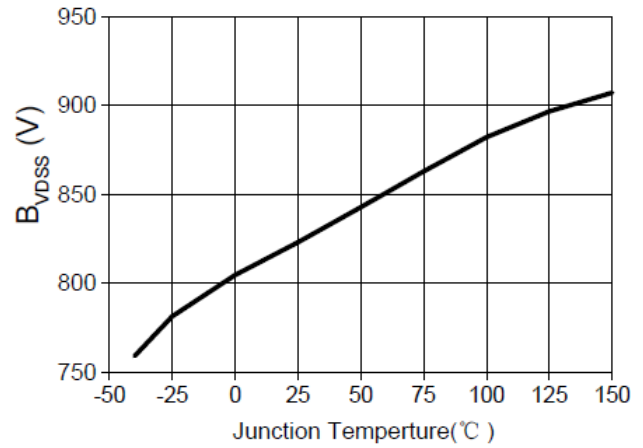


TYPICAL PERFORMANCE CHARACTERISTICS

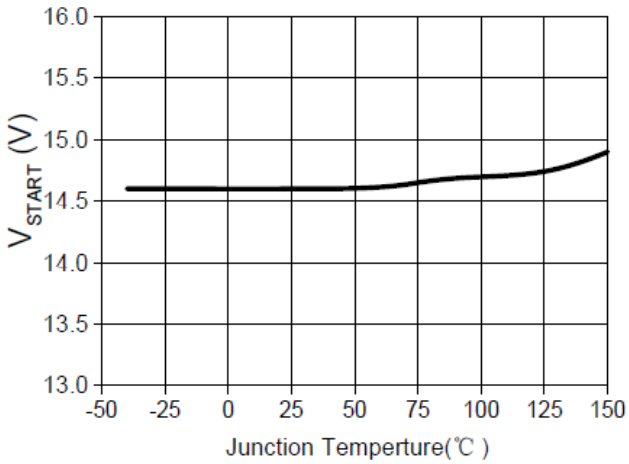
1. $R_{DS(on)}$ vs. T_J



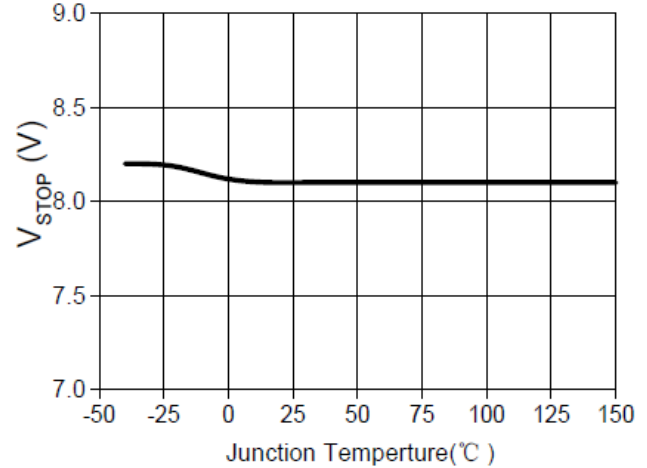
2. B_{VDSS} vs. T_J



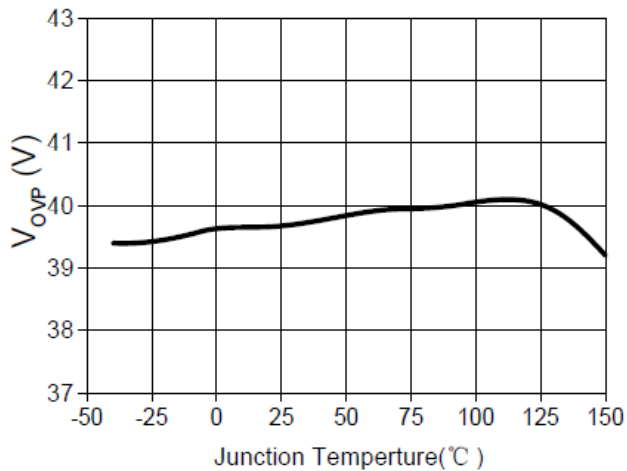
3. V_{START} vs. T_J



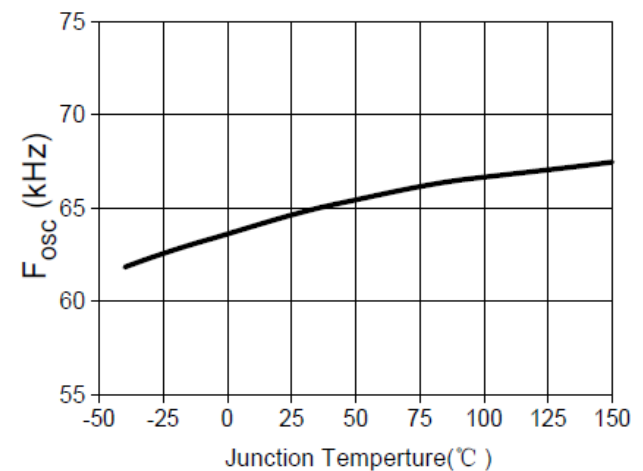
4. V_{STOP} vs. T_J



5. V_{OVP} vs. T_J



6. F_{osc} vs. T_J





DETAILED INFORMATION

Functional Description

Startup

This device includes a high voltage start up current source connected on the SW of the device. As soon as a voltage is applied on the input of the converter, this start up current source is activated and to charge the V_{DD} capacitor as long as V_{DD} is lower than V_{START} . When reaching V_{START} , the start up current source is cut off and V_{DD} is sourced by auxiliary side. As V_{DD} falls below V_{STOP} , the HV-Start circuit won't work immediately until V_{DD} is lower than V_{RST} .

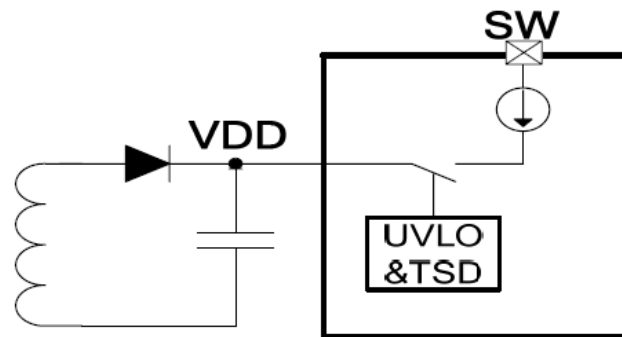


Fig 1. Startup circuit

Soft-start up

In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and help to prevent the transformer turning into the saturation states. Typically, the duration of soft-start is 7.5ms.

Gate driver

The internal power MOSFET in AP8022 is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in worse EMI.

A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

Oscillator

The switching frequency of AP8022 is internally fixed at 60 kHz. No external frequency setting components are required for PCB design.

The frequency modulation is implemented in AP8022. So that, it minimizes the conduction band EMI and therefore eases the system design because the tone energy could be spread out.



Feed-back

A feedback pin controls the operation of the device. Unlike conventional PWM control circuits which use a voltage input, the COMP pin is sensitive to current. Fig. 2 presents the internal current mode structure. The Power MOSFET delivers a sense current which is proportional to the main current. R2 receives this current and the current coming from the COMP pin. The voltage across R2 (V_{R2}) is then compared to a fixed reference voltage. The MOSFET is switched off when V_{R2} equals the reference voltage.

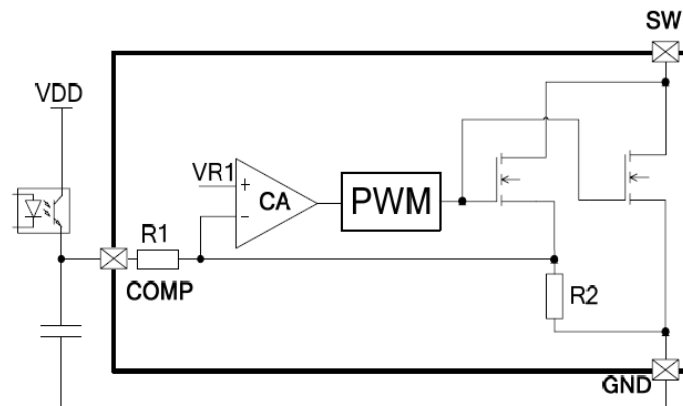


Fig 2. Feedback circuit

Leading Edge Blanking (LEB)

At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by the primary side capacitance and secondary side rectifier diode reverse recovery. Excessive voltage across the sense resistor would lead to false feedback operation in the current mode PWM control. To counter this effect, the device employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (typically 650ns) after the Sense FET is turned on.

Under Voltage Lock Out

Once fault condition occurs, switching is terminated and the Sense FET remains off. This causes V_{DD} to fall. When V_{DD} reaches the V_{DD} reset voltage, 6V, the protection is reset and the internal high voltage current source charges the V_{DD} capacitor. When V_{DD} reaches the UVLO start voltage, 14.5V, the device resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

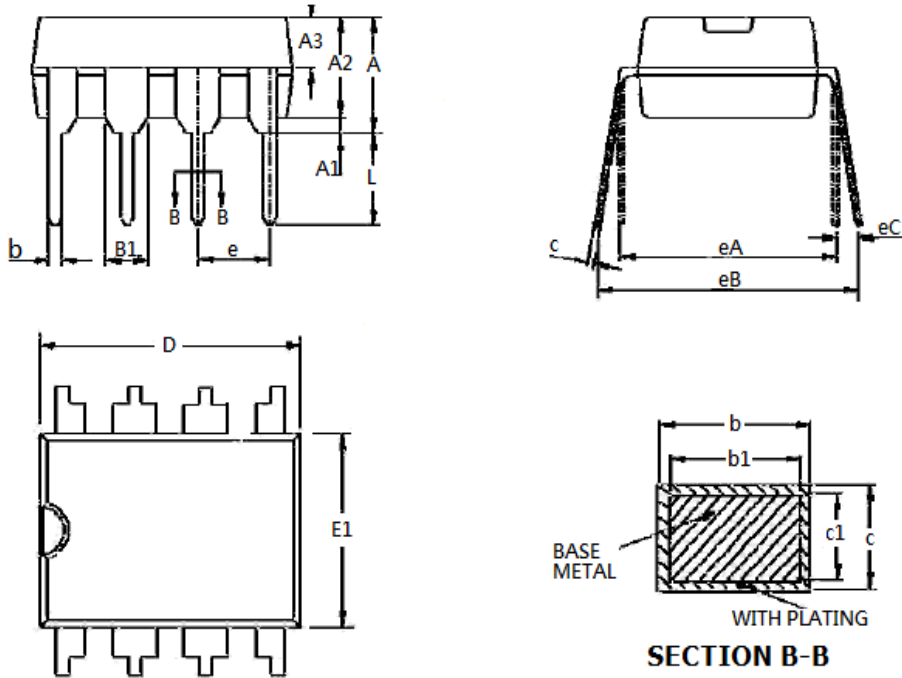
Thermal Shutdown (TSD)

The Sense FET and the control IC are integrated in the same chip, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 170°C, thermal shutdown is activated, the device turn off the Sense FET. The device will go back to work when the lower threshold temperature about 140°C is reached.



PACKAGE INFORMATION

Dimension in DIP8 (Unit: mm)



Symbol	Min	Max
A	3.60	4.00
A1	0.51	-
A2	3.00	3.40
A3	1.55	1.65
b	0.44	0.53
b1	0.43	0.48
B1	1.52BSC	
c	0.24	0.32
c1	0.23	0.27
D	9.05	9.45
E1	6.15	6.55
e	2.54BSC	
eA	7.62BSC	
eB	7.62	9.30
eC	0.00	0.84
L	3.00	-



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