



# FQP12N60C/FQPF12N60C

## 600V N-Channel MOSFET

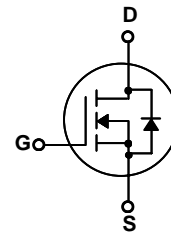
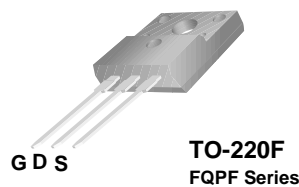
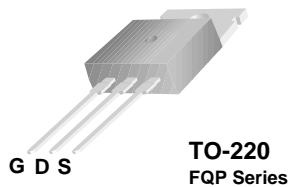
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Corise Semiconductor's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

### Features

- 12A, 600V,  $R_{DS(on)} = 0.65\Omega$  @  $V_{GS} = 10V$
- Low gate charge ( typical 48 nC)
- Low  $C_{rss}$  ( typical 21 pF)
- Fast switching
- 100% avalanche tested
- Improved  $dv/dt$  capability



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQP12N60C	FQPF12N60C	Units
$V_{DSS}$	Drain-Source Voltage	600		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	12	12 *	A
		7.4	7.4 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	48	48 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	870		mJ
$I_{AR}$	Avalanche Current (Note 1)	12		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	22.5		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	225	51	W
		1.78	0.41	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FQP12N60C	FQPF12N60C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.56	2.43	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to 25°C	--	0.5	--	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	--	0.53	0.65	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 6\text{ A}$ (Note 4)	--	13	--	S

<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1760	2290	pF
$C_{oss}$	Output Capacitance		--	182	235	pF
$C_{riss}$	Reverse Transfer Capacitance		--	21	28	pF

<b>Switching Characteristics</b>							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 12\text{ A},$ $R_G = 25\ \Omega$	--	30	70	ns	
$t_r$	Turn-On Rise Time		--	85	180	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	155	120	ns
$t_f$	Turn-Off Fall Time			--	90	190	ns
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 10\text{ V}$	--	48	63	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4, 5)	--	8.5		nC
$Q_{gd}$	Gate-Drain Charge			--	21		nC

<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	12		A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	48		A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 12\text{ A},$	--	420	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	4.9	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 11\text{ mH}, I_{AS} = 12\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 12\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

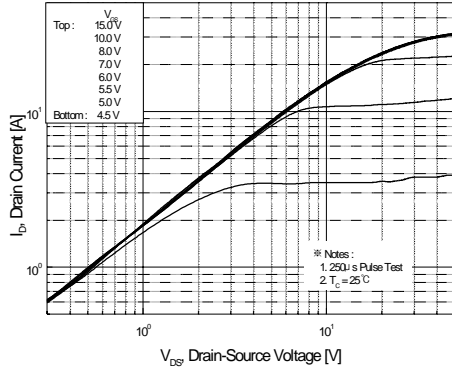


Figure 1. On-Region Characteristics

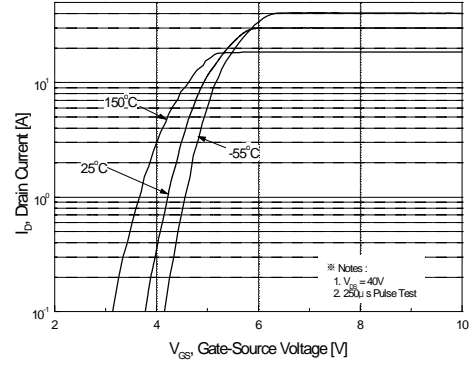


Figure 2. Transfer Characteristics

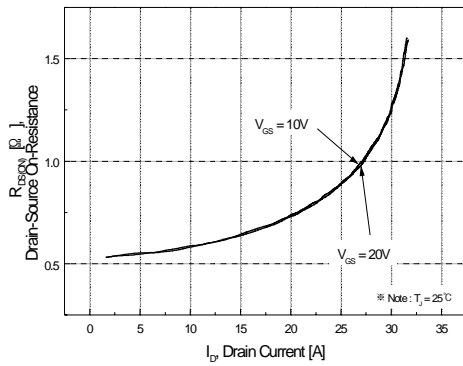


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

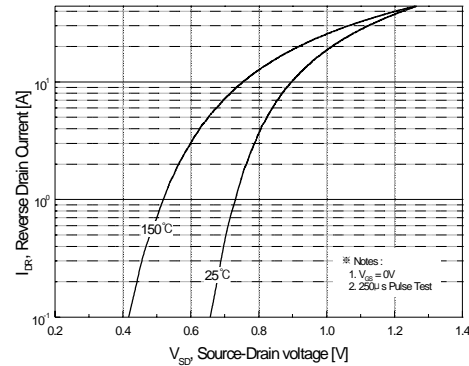


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

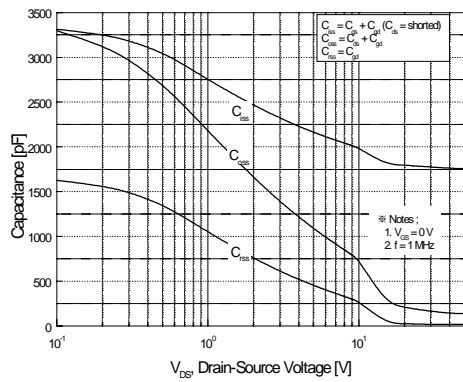


Figure 5. Capacitance Characteristics

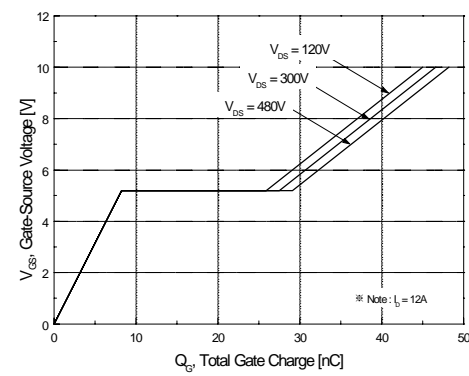


Figure 6. Gate Charge Characteristics

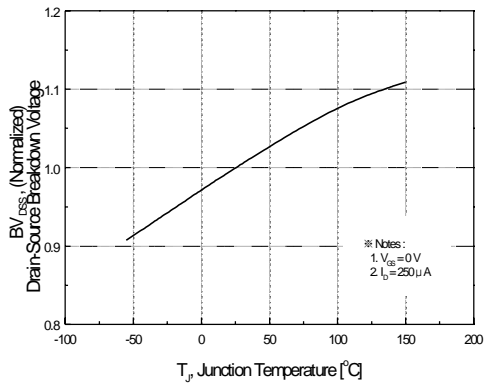


Figure 7. Breakdown Voltage Variation vs Temperature

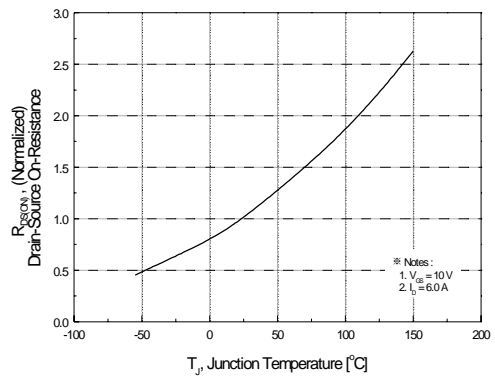


Figure 8. On-Resistance Variation vs Temperature

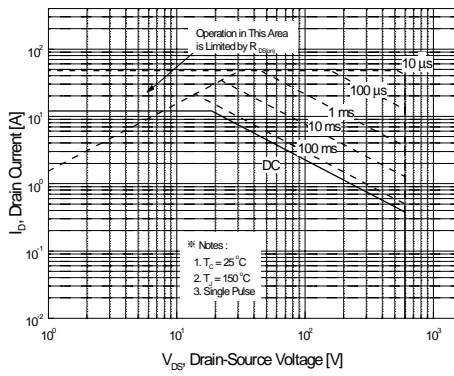


Figure 9-1. Maximum Safe Operating Area for FQP12N60C

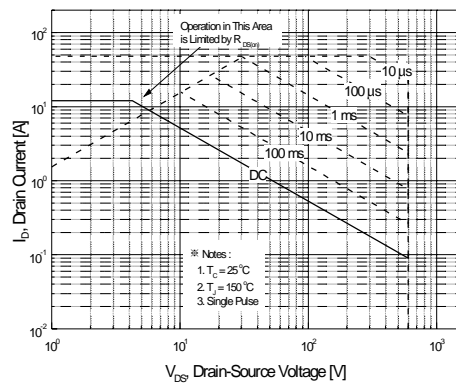


Figure 9-2. Maximum Safe Operating Area for FQPF12N60C

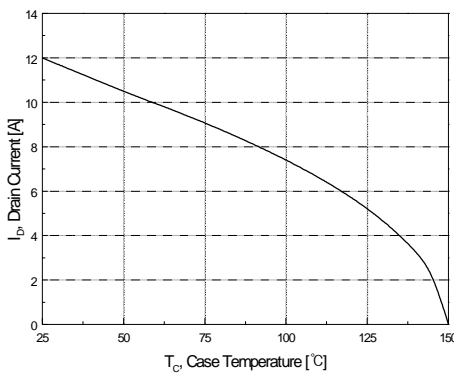


Figure 10. Maximum Drain Current vs Case Temperature

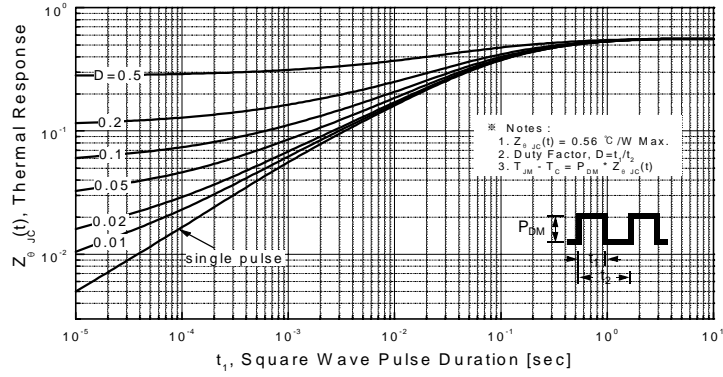


Figure 11-1. Transient Thermal Response Curve for FQP12N60C

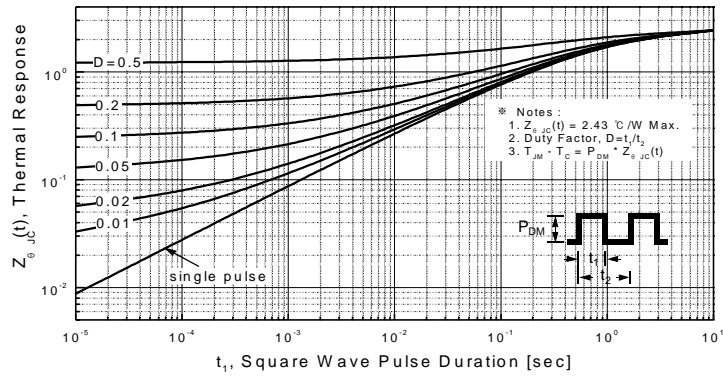
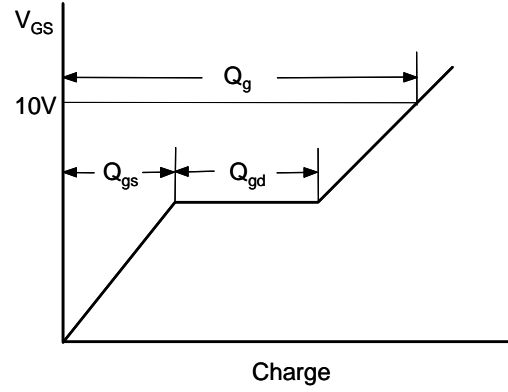
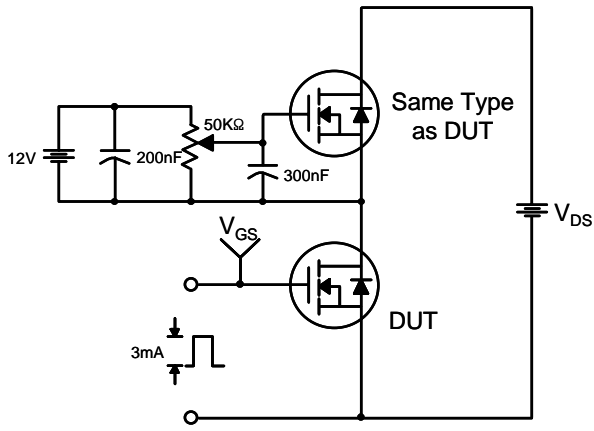
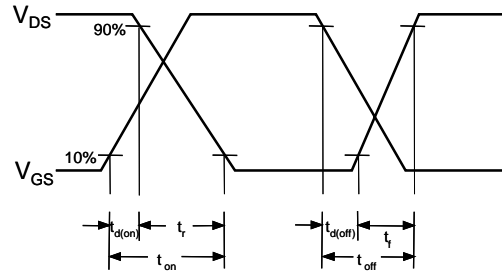
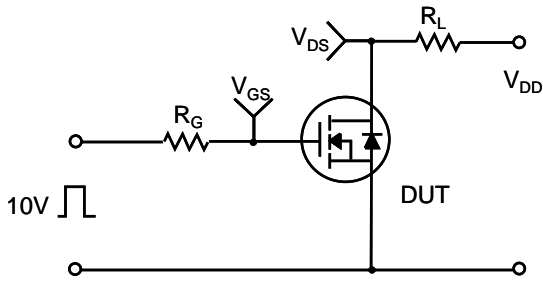


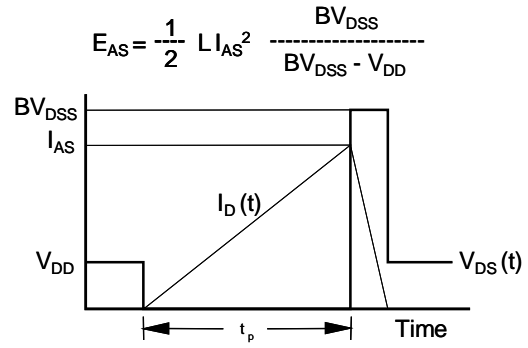
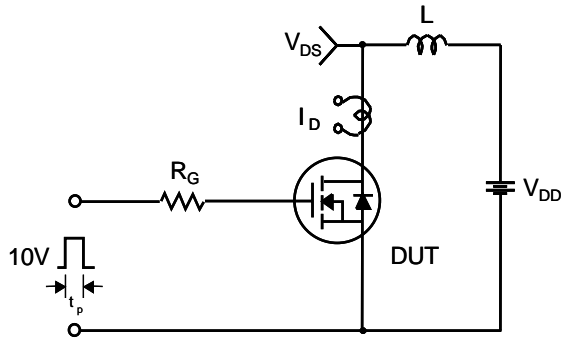
Figure 11-2. Transient Thermal Response Curve for FQPF12N60C

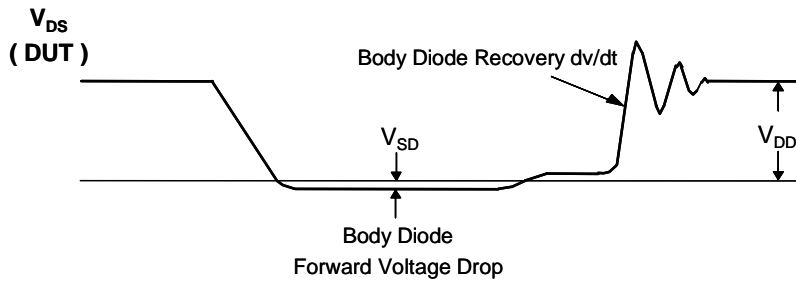
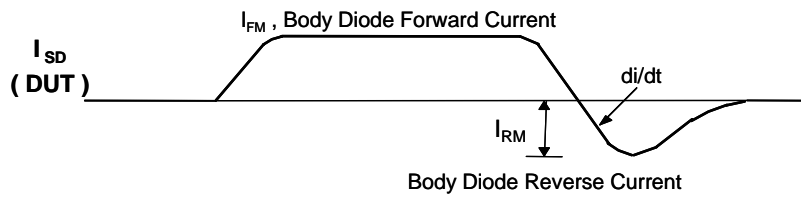
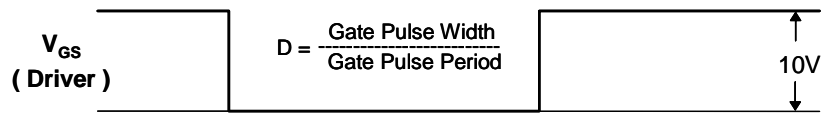
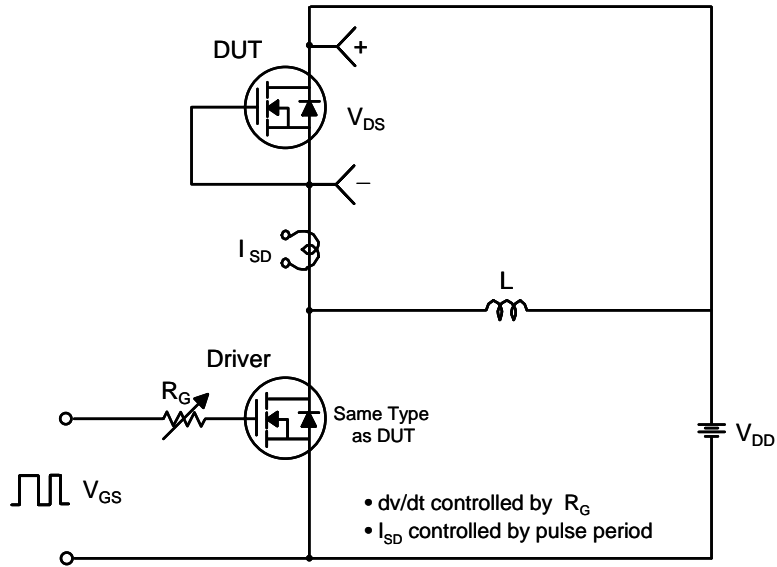


Resistive Switching Test Circuit & Waveforms

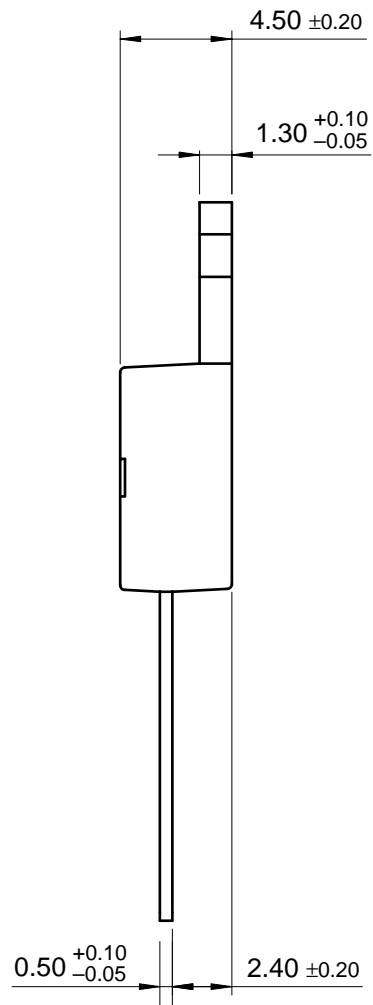
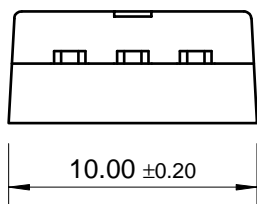
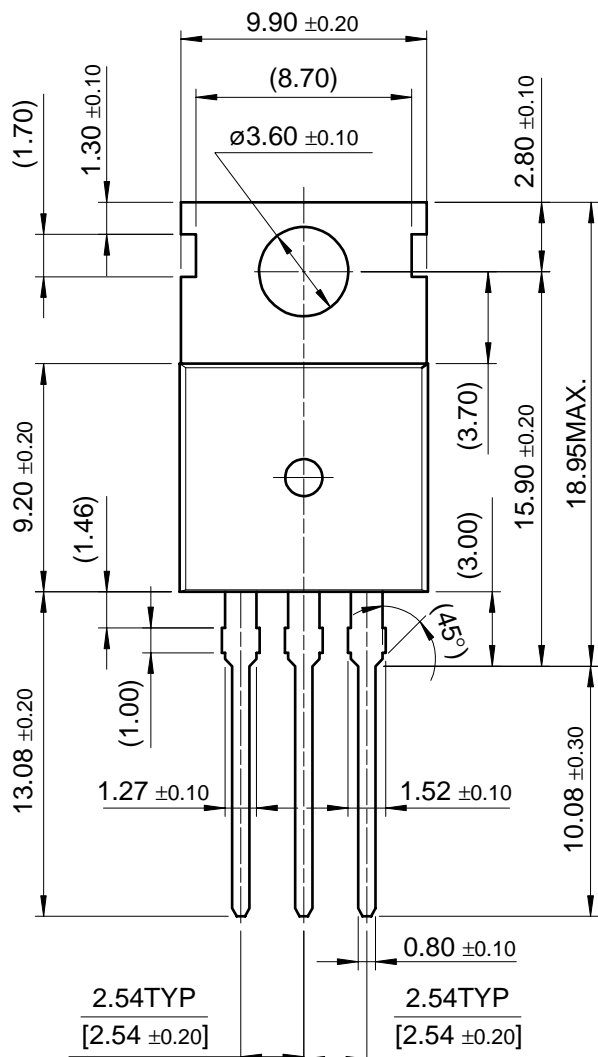


Unclamped Inductive Switching Test Circuit & Waveforms





# TO-220



FQP12N60C/FQPF12N60C



# TO-220F

