

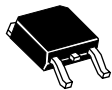


Power MOSFET

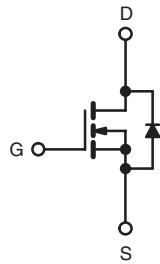
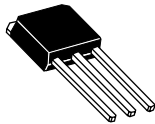
PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	3.0
Q_g (Max.) (nC)	17	
Q_{gs} (nC)	4.3	
Q_{gd} (nC)	8.5	
Configuration	Single	

DPAK
(TO-252)



IPAK
(TO-251)



N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{OSS} Specified
- Lead (Pb)-free Available



RoHS*
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR420APbF	IRFR420ATRLPbF ^a	IRFR420ATRLPbF	IRFU420APbF
	SiHFR420A-E3	SiHFR420AT-E3 ^a	SiHFR420ATL-E3	SiHFU420A-E3
SnPb	IRFR420A	-	-	IRFU420A
	SiHFR420A	-	-	SiHFU420A

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	3.3	A
		2.1	
Pulsed Drain Current ^a	I_{DM}	10	
Linear Derating Factor		0.67	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	140	mJ
Repetitive Avalanche Current ^a	I_{AR}	2.5	A
Repetitive Avalanche Energy ^a	E_{AR}	5.0	mJ
Maximum Power Dissipation	P_D	83	W
Peak Diode Recovery dV/dt ^c	dV/dt	3.4	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 45\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 2.5\text{ A}$ (see fig. 12).
- $I_{SD} \leq 2.5\text{ A}$, $dI/dt \leq 270\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.5	

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.60	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.5\text{ A}^b$	-	-	3.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 1.5\text{ A}$		1.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	340	-	pF
Output Capacitance	C_{oss}			-	53	-	
Reverse Transfer Capacitance	C_{rss}			-	2.7	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	490	-	pF
			$V_{DS} = 400\text{ V}$, $f = 1.0\text{ MHz}$	-	15	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	28	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 2.5\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	17	nC
Gate-Source Charge	Q_{gs}			-	-	4.3	
Gate-Drain Charge	Q_{gd}			-	-	8.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 21\text{ }\Omega$, $R_D = 97\text{ }\Omega$, see fig. 10 ^b		-	8.1	-	ns
Rise Time	t_r			-	12	-	
Turn-Off Delay Time	$t_{d(off)}$			-	16	-	
Fall Time	t_f			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	3.3	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	10	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 2.5\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 2.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	330	500	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	760	1140	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .



KERSEMI

IRFR420A, IRFU420A, SiHFR420A,

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

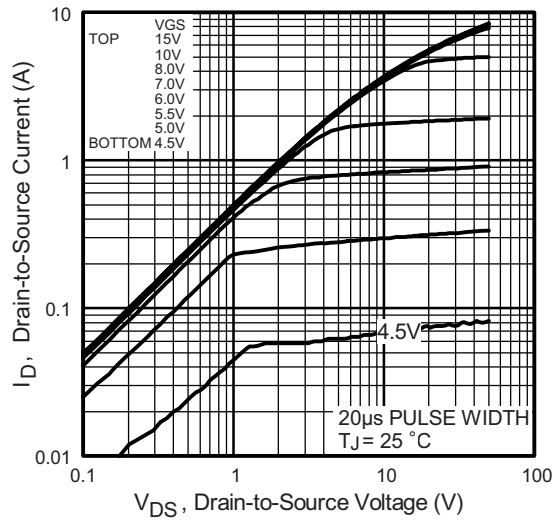


Fig. 1 - Typical Output Characteristics

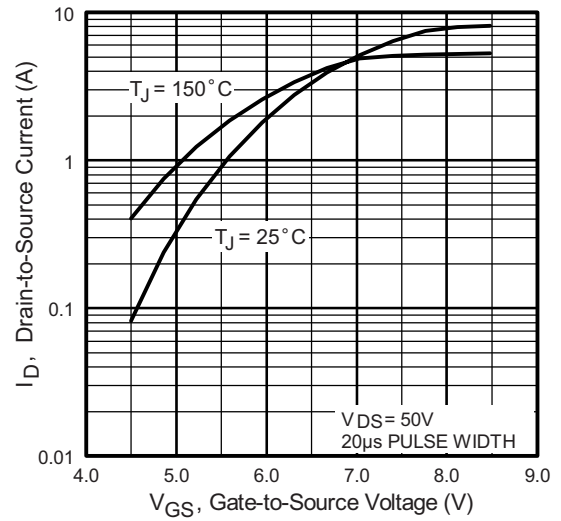


Fig. 3 - Typical Transfer Characteristics

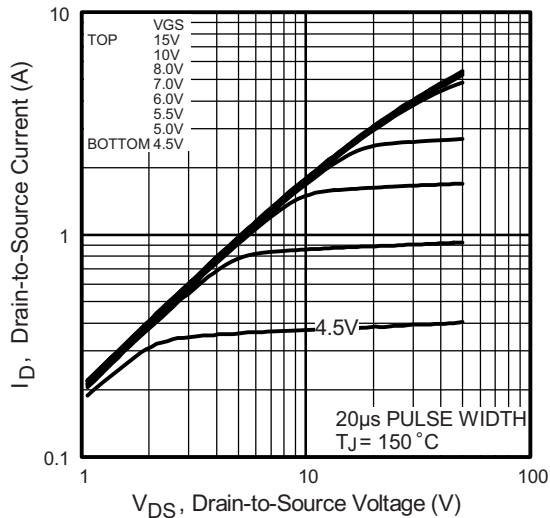


Fig. 2 - Typical Output Characteristics

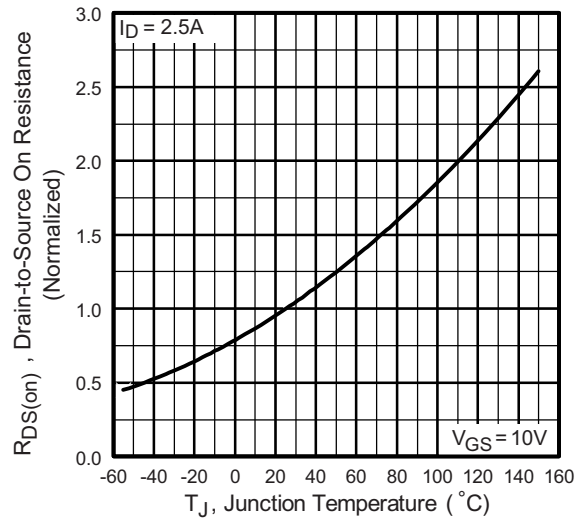


Fig. 4 - Normalized On-Resistance vs. Temperature

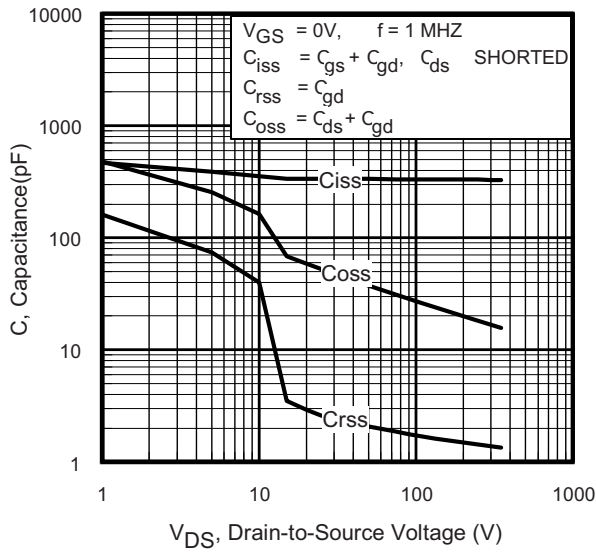


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

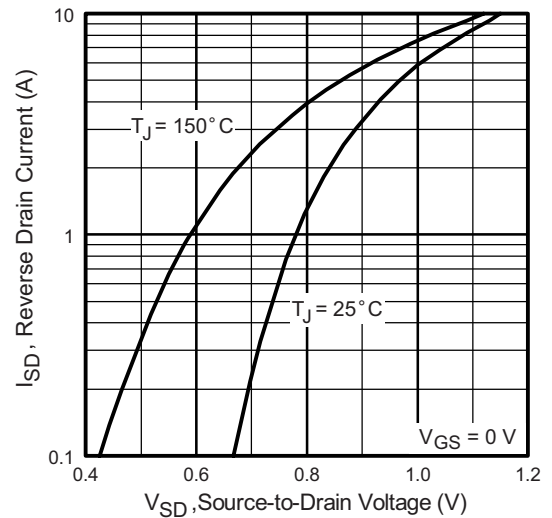


Fig. 7 - Typical Source-Drain Diode Forward Voltage

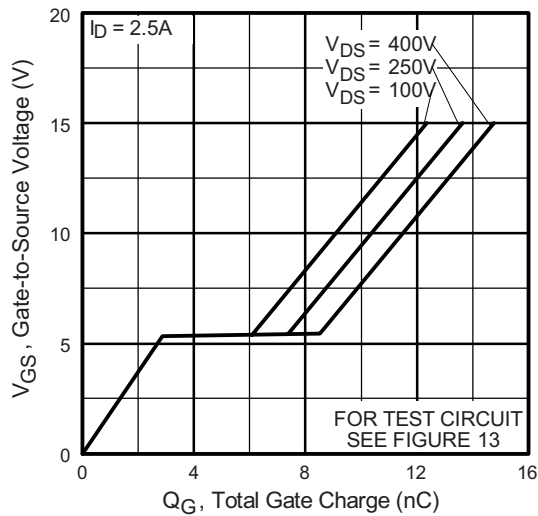


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

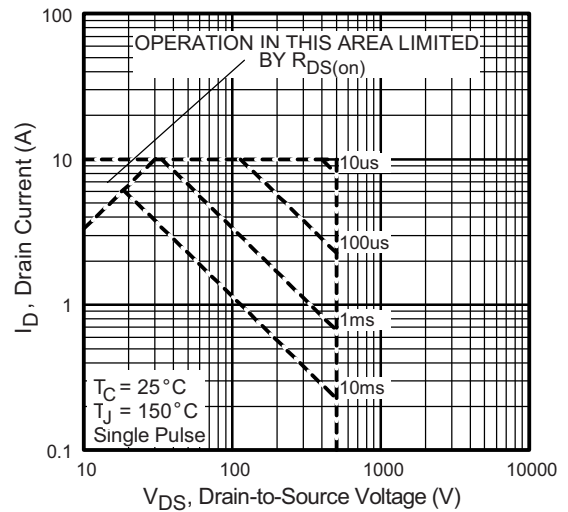


Fig. 8 - Maximum Safe Operating Area

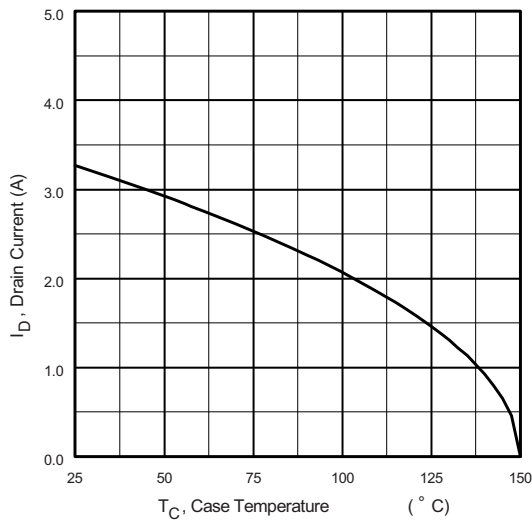


Fig. 9 - Maximum Drain Current vs. Case Temperature

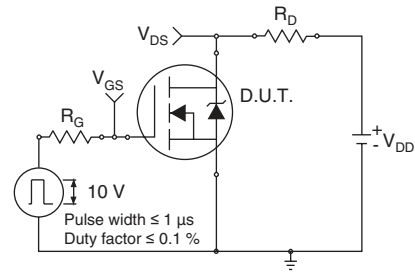


Fig. 10a - Switching Time Test Circuit

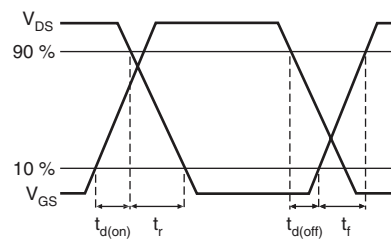


Fig. 10b - Switching Time Waveforms

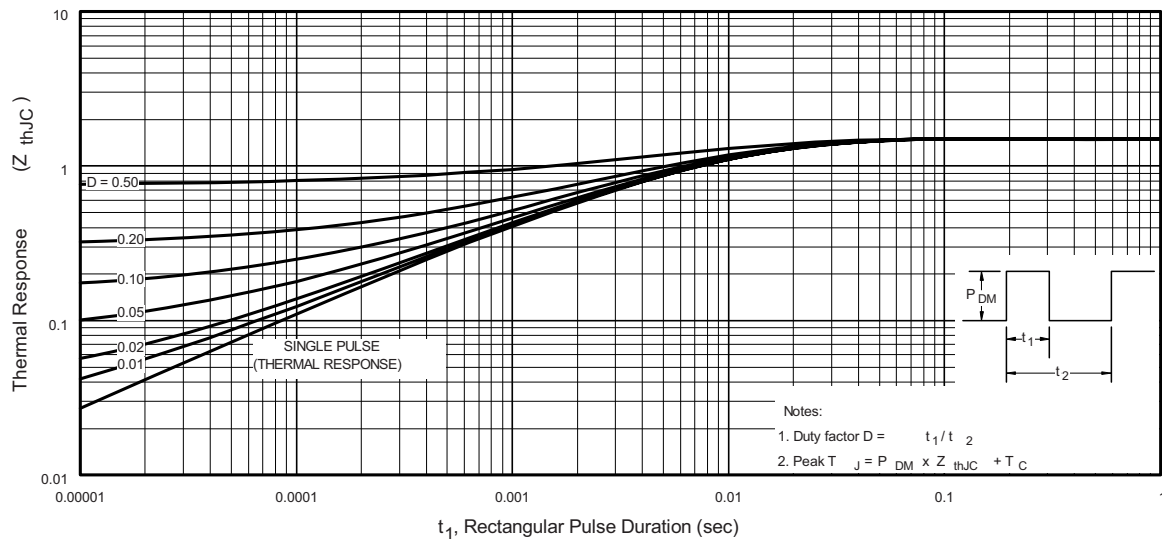


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

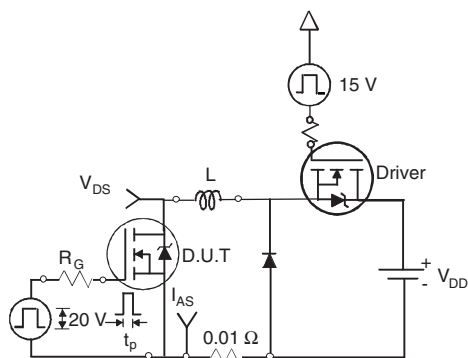


Fig. 12a - Unclamped Inductive Test Circuit

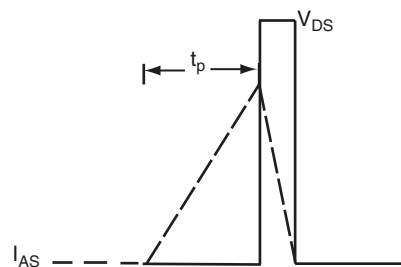


Fig. 12b - Unclamped Inductive Waveforms

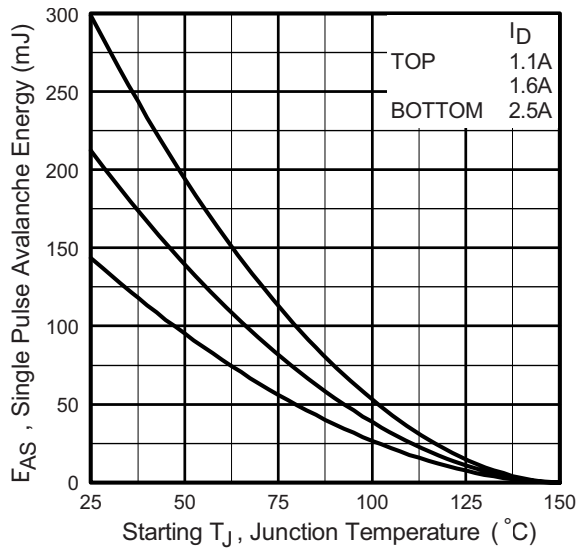


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

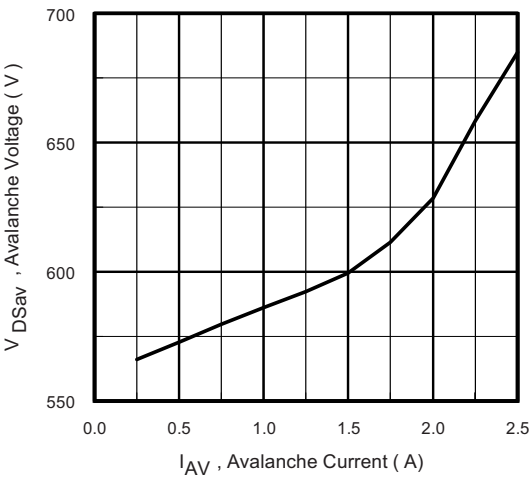


Fig. 12d - Maximum Avalanche Energy vs. Drain Current

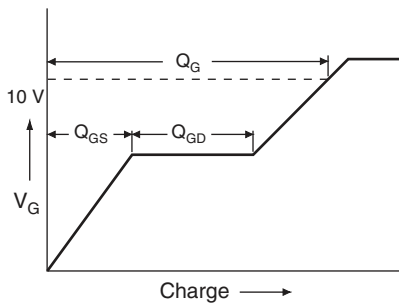


Fig. 13a - Basic Gate Charge Waveform

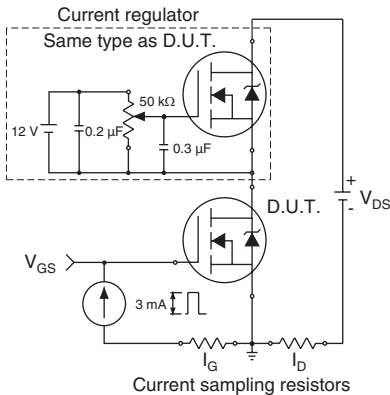
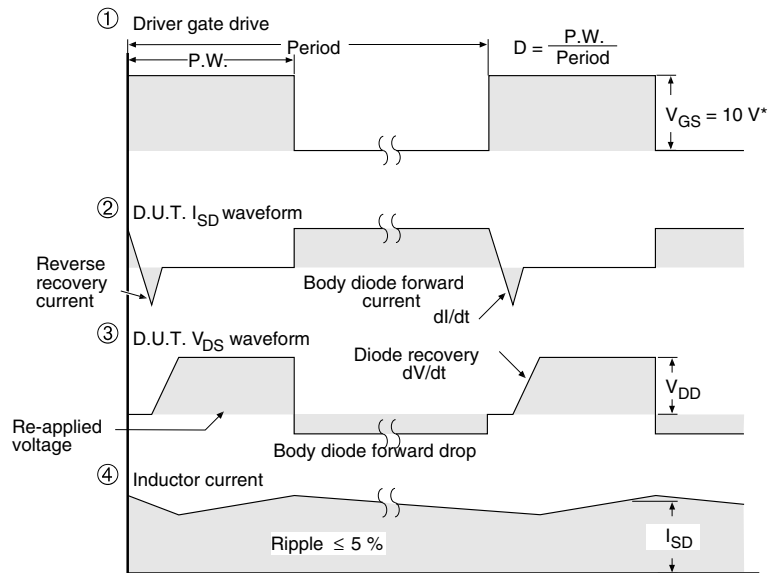
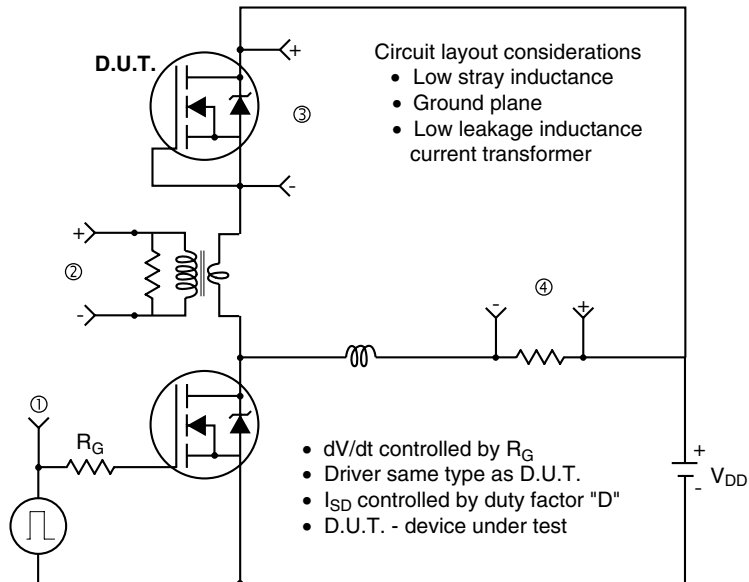


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel